ANNA UNIVERSITY TIRUCHIRAPPALLI
Tiruchirappalli – 620 024
Regulations 2008
Curriculum

M.E. VLSI DESIGN

SEMESTER I

S.No.	Subject Code	Subject	L	T	P	C
Theory						
1	**MA 5131**	Applied Mathematics for Electronics Engineers	3	1	0	4
2	**VL5101**	Digital Signal Processing Integrated Circuits	3	0	0	3
3	**AN5102**	Advanced Digital System Design	3	1	0	4
4	**AN5103**	VLSI Design Techniques	3	0	0	3
5	**VL5102**	Solid State Device Modeling and Simulation	3	0	0	3
6	**E1******	Elective I	3	0	0	3
Practical						
7	**VL5103**	VLSI Design Laboratory I	0	0	4	3
					Total	**23**

SEMESTER II

S.No.	Subject Code	Subject	L	T	P	C
Theory						
1	**AN 5151**	Analysis and Design of Analog Integrated Circuits	3	0	0	3
2	**VL 5151**	Computer Aided Design of VLSI Circuits	3	0	0	3
3	**AN 5152**	Computer Architecture and Parallel Processing	3	0	0	3
4	**AN 5154**	Embedded Systems	3	0	0	3
5	**E2******	Elective II	3	0	0	3
6	**E3******	Elective III	3	0	0	3
Practical						
7	**VL 5152**	VLSI Design Laboratory II	0	0	4	3
					Total	**21**

SEMESTER III

S.No.	Subject Code	Subject	L	T	P	C
Theory						
1	**E4******	Elective IV	3	0	0	3
2	**E5******	Elective V	3	0	0	3
3	**E6******	Elective VI	3	0	0	3
Practical						
4	**VL5251**	Project Work Phase I	0	0	12	6
					Total	**15**

SEMESTER IV

S.No.	Subject Code	Subject	L	T	P	C
Practical						
1	**VL5251**	Project Work Phase II	0	0	24	12
					Total	**12**

Total Credits to be Earned for the Award of the Degree = 71

LIST OF ELECTIVES

S.No.	Subject Code	Subject	L	T	P	C
Theory						
1	**VL5001**	Testing of VLSI Circuits	3	0	0	3
2	**VL5002**	Low Power VLSI Design	3	0	0	3
3	**VL5003**	VLSI Signal Processing	3	0	0	3
4	**VL5004**	CMOS VLSI Design	3	0	0	3
5	**VL5005**	Analog VLSI Design	3	0	0	3
6	**VL5006**	Design of Semiconductor Memories	3	0	0	3
7	**VL5007**	VLSI Technology	3	0	0	3
8	**VL5008**	Physical Design of VLSI Circuits	3	0	0	3
9	**VL5009**	Genetic Algorithms and their Applications	3	0	0	3
10	**AN5104**	Advanced Microprocessors and Microcontrollers	3	0	0	3
11	**AN5002**	Neural Networks and Applications	3	0	0	3
12	**AN5005**	ASIC Design	3	0	0	3
13	**AN5007**	Reliability Engineering	3	0	0	3
14	**AN5009**	Electromagnetic Interference and Compatibility in System Design	3	0	0	3
15	**CO5006**	Speech and Audio Signal Processing	3	0	0	3
16	**CO5004**	DSP Processor Architecture and Programming	3	0	0	3
17	**VL 5025**	Special Elective	3	0	0	3

ANNA UNIVERSITY TIRUCHIRAPPALLI

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Regulations 2008

Sylllabus

M.E. VLSI DESIGN

SEMESTER I

MA5131 – APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS

L	T	P	C
3	1	0	4

UNIT I LINEAR ALGEBRAIC EQUATIONS & EIGEN VALUE PROBLEMS 9

System of Equations – Solutions by Gauss Elimination Methods – Gauss Jordan and LU Decomposition Method Jacobi – Gauss Seidel Method – Eigen Values of Matrix by Jacobi and Power Method.

UNIT II THE WAVE EQUATIONS 9

Solution of Initial and Boundary Value Problems – Characteristics–D'Alembert's Solution– Significance of Characteristic Curves – Laplace Transform Solutions – for Displacement in a Long String – A long String under its Weight – Longitudinal Vibration of a Elastic Bar with Prescribed Force on one end – Free Vibrations of a String .

UNIT III SPECIAL FUNCTIONS 9

Bessel's Equation – Bessel Functions Legendre's Equation – Legendre Polynomials Rodrigue's Formula – Recurrence Relations – Generating Functions and Orthogonal Property for Bessel Functions – Legendre Polynomials.

UNIT IV RANDOM VARIABLES 9

One–Dimensional Random Variables – Moments and Moment Generating Function –Binomial Poisson– Uniform – Exponential Normal and Weibull Distribution – Two Dimensional Random Variables Marginal and Conditional Distribution Covariance – Correlation Coefficient – Function of One Dimensional and Two Dimensional Random Variables.

UNIT V QUEUING THEORY 9

Single and Multiple Server Markovian Queuing Models – Steady State System Size Probabilities– Little's Formula – Customer Impatience Priority Queues – M/G/1 Queuing System – PK Formula .

L: 45 T: 15 Total: 60

TEXT BOOKS

1. S. Narayanan T. K. Manichvachagam Pillay and G. Ramanaiah, "Advanced Mathematics for Engineering Students", S.Viswanathan Pvt Ltd, Vol 2, 1986.
2. Taha H. A., "Operations Research An Introduction", Sixth Edition, PHI, 1997.

REFERENCES

1. Sankara Rao K, "Introduction to Partial Differential Equation", PHI, 1995.
2. Churchi R. V., "Operational Mathematics", McGraw Hill, 1972.
3. Richard A. Johnson, "Miller and Freund's Probability and Statistics for Engineers", Fifth Edition, PHI, 1994.

VL5101 – DIGITAL SIGNAL PROCESSING INTEGRATED CIRCUITS

L	T	P	C
3	0	0	3

UNIT I DSP INTEGRATED CIRCUITS AND VLSI CIRCUIT TECHNOLOGIES 9

Standard digital signal processors – Application specific IC's for DSP – DSP systems – DSP system design – Integrated circuit design – MOS transistors – MOS logic – VLSI process technologies – Trends in CMOS technologies

UNIT II DIGITAL SIGNAL PROCESSING 9

Digital signal processing – Sampling of analog signals – Selection of sample frequency – Signal – processing systems – Frequency response – Transfer functions – Signal flow graphs – Filter structures – Adaptive DSP algorithms – DFT – The Discrete Fourier Transform – FFT – The Fast Fourier Transform Algorithm – Image coding – Discrete Cosine Transforms

UNIT III DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS 9

FIR filters – FIR filter structures – FIR chips – IIR filters – Specifications of IIR filters – Mapping of analog transfer functions – Mapping of analog filter structures – Multirate systems – Interpolation with an integer factor L– Sampling rate change with a ratio L/M– Multirate filters – Finite word length effects – Parasitic oscillations – Scaling of signal levels – Round–off noise – Measuring round–off noise – Coefficient sensitivity – Sensitivity and noise

UNIT IV DSP ARCHITECTURES AND SYNTHESIS OF DSP ARCHITECTURES 9

DSP system architectures – Standard DSP architecture – Ideal DSP architectures – Multiprocessors and multicomputers – Systolic and Wave front arrays – Shared memory architectures Mapping of DSP algorithms onto hardware – Implementation based on complex PEs – Shared memory architecture with Bit – serial PEs

UNIT V ARITHMETIC UNITS AND INTEGRATED CIRCUIT DESIGN 9

Conventional number system – Redundant Number system – Residue Number System Bit–parallel and Bit–Serial arithmetic – Basic shift accumulator – Reducing the memory size – Complex multipliers – Improved shift–accumulator Layout of VLSI circuits – FFT processor – DCT processor and Interpolator as case studies

Total: 45

TEXT BOOKS

1. Lars Wanhammer, **"**DSP Integrated Circuits**"**, Academic Press, New York 1999.
2. Keshab K.Parhi, "VLSI digital Signal Processing Systems design and Implementation", John Wiley and Sons, 1999.

REFERENCES

1. A.V. Oppenheim et.al., "Discrete-time Signal Processing", Pearson Education, 2000.
2. Emmanuel C. Ifeachor- Barrie W. Jervis- **"** Digital signal processing - A practical approach**",** 2nd edition, Pearson Education, 2001.
3. A.V. Oppenheim and Ronald Wischafer, "Digital Signal Processing", 1975.
4. B. Venkataramani, M. Bhaskar, "Digital Signal Processors: Architecture Programming and Application", Mc Graw Hill Publishing Company Limited, 2003.

AN5102 – ADVANCED DIGITAL SYSTEM DESIGN

L	T	P	C
3	1	0	4

UNIT I SEQUENTIAL CIRCUIT DESIGN 9

Analysis of Clocked Synchronous Sequential Networks (CSSN) Modeling of CSSN – State Stable Assignment and Reduction – Design of CSSN – Design of Iterative Circuits – ASM Chart – ASM Realization

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9

Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC – State Assignment – Problem and the Transition Table – Design of ASC – Static and Dynamic Hazards – Essential Hazards – Data Synchronizers – Designing Vending Machine Controller – Mixed Operating Mode Asynchronous Circuits

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

Fault Table Method – Path Sensitization Method – Boolean Difference Method – Kohavi Algorithm – Tolerance Techniques – The Compact Algorithm – Practical PLA's – Fault in PLA – Test Generation – Masking Cycle – DFT Schemes – Built–in Self Test

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9

EPROM to Realize a Sequential Circuit – Programmable Logic Devices – Designing a Synchronous Sequential Circuit using a GAL – EPROM – Realization State machine using PLD – FPGA – Xilinx FPGA – Xilinx 2000 – Xilinx 3000

UNIT V SYSTEM DESIGN USING VHDL 9

VHDL Description of Combinational Circuits – Arrays – VHDL Operators – Compilation and Simulation of VHDL Code – Modeling using VHDL – Flip Flops – Registers – Counters – Sequential Machine – Combinational Logic Circuits – VHDL Code for – Serial Adder– Binary Multiplier – Binary Divider – Complete Sequential Systems – Design of a Simple Microprocessor

L: 45 T: 15 Total: 60

TEXT BOOKS

1. Donald G. Givone "Digital principles and Design" Tata McGraw Hill 2002.
2. John M Yarbrough "Digital Logic applications and Design", Thomson Learning, 2001

REFERENCES

1. Nripendra N Biswas, "Logic Design Theory", Prentice Hall of India, 2001
2. Charles H. Roth Jr., "Digital System Design using VHDL", Thomson Learning, 1998.
3. Charles H. Roth Jr., "Fundamentals of Logic design", Thomson Learning- 2004.
4. Stephen Brown and Zvonk Vranesic, "Fundamentals of Digital Logic with VHDL Design", Tata McGraw Hill, 2002.

AN5103 – VLSI DESIGN TECHNIQUES

L	T	P	C
3	0	0	3

UNIT I MOS TRANSISTOR THEORY AND PROCESS TECHNOLOGY 9

NMOS and PMOS transistors – Threshold voltage – Body effect – Design equations– Second order effects – MOS models and small signal AC characteristics – Basic CMOS technology

UNIT II INVERTERS AND LOGIC GATES 9

NMOS and CMOS Inverters – Stick diagram – Inverter ratio – DC and transient characteristics – Switching times – Super buffers – Driving large capacitance loads – CMOS logic structures – Transmission gates – Static CMOS design – Dynamic CMOS design

UNIT III CIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION 9

Resistance estimation – Capacitance estimation – Inductance – switching characteristics – transistor sizing – power dissipation and design margining – Charge sharing – Scaling

UNIT IV VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN 9

Multiplexers – Decoders – comparators – priority encoders – Shift registers –Arithmetic circuits – Ripple carry adders – Carry look ahead adders – High–speed adders – Multipliers – Physical design – Delay modeling – Cross talk – Floor planning – power distribution – Clock distribution – Basics of CMOS testing

UNIT V VERILOG HARDWARE DESCRIPTION 9

Overview of digital design with Verilog HDL – Hierarchical modeling concepts– modules and port definitions – Gate level modeling– data flow modeling – behavioral modeling – Task & Functions – Test Bench

Total: 45

TEXT BOOKS

1. Neil H.E. Weste and Kamran Eshraghian, “Principles of CMOS VLSI Design”, Pearson Education, 2nd Edition, 2000.
2. Samir Palnitkar, “Verilog HDL”, Pearson Education, 2nd Edition, 2004.

REFERENCES

1. John P.Uyemura “Introduction to VLSI Circuits and Systems”, John Wiley and Sons, Inc., 2002.
2. Eugene D.Fabricius- Introduction to VLSI Design McGraw Hill International Editions- 1990.
3. J.Bhasker- B.S.Publications- “A Verilog HDL Primer”- 2nd Edition- 2001.
4. Pucknell- “Basic VLSI Design”- Prentice Hall of India Publication- 1995.
5. Wayne Wolf “Modern VLSI Design System on chip. Pearson Education.2002.

VL5102 – SOLID STATE DEVICE MODELING AND SIMULATION

L	T	P	C
3	0	0	3

UNIT I BASIC SEMICONDUCTOR PHYSICS 9

Quantum Mechanical Concepts – Carrier Concentration – Transport Equation – Bandgap – Mobility and Resistivity – Carrier Generation and Recombination – Avalanche Process – Noise Sources

UNIT II BIPOLAR DEVICE MODELING 9

Injection and Transport Model – Continuity Equation – Diode Small Signal and Large Signal (Change Control Model) – Transistor Models: Ebber – Molls and Gummel Port Model – Mextram model – SPICE modeling temperature and area effects

UNIT III MOSFET MODELING 9

Introduction Interior Layer – MOS Transistor Current – Threshold Voltage – Temperature Short Channel and Narrow Width Effect – Models for Enhancement – Depletion Type MOSFET – CMOS Models in SPICE

UNIT IV PARAMETER MEASUREMENT 9

General Methods – Specific Bipolar Measurement – Depletion Capacitance – Series Resistances – Early Effect – Gummel Plots – MOSFET: Long and Short Channel Parameters – Statistical Modeling of Biopolar and MOS Transistors

UNIT V OPTOELECTRONIC DEVICE MODELING 9

Static and Dynamic Models – Rate Equations – Numerical Technique – Equivalent Circuits – Modeling of LEDs – Laser Diode and Photo detectors

Total: 45

TEXT BOOKS

1. Philip E. Allen- Douglas R.Hoberg- “CMOS Analog Circuit Design” Second Edition-OxfordPress - 2002.
2. Tor A. Fjeldly, Trond Ytterdal, Michaels Shur, “Introduction to Device Modeling and CircuitSimulation”, John Wiley & sons, Inc, 1998

REFERENCES

1. Kiat Seng Yeo, Samir S.Rofail, Wang,Ling Gob, “CMOS / BiCMOS ULSI - Low Voltage,Low Power”, Person education, Low price edition, 2003.
2. S.M.Sze, “Semiconductor Devices - Physics and Technology”, John Wiley and sons, 1985.
3. Giuseppe Massobrio and Paolo Antogentti,“Semiconductor Device Modeling with SPICE”, Second Edition, McGraw Hill Inc., 1993.
4. Mohammed Ismail and Terri Fiez, “Analog VLSI-Signal and Information Processing”, 1st Edition, Tata McGraw Hill Publishing company Ltd., 2001

VL5103 – VLSI DESIGN LABORATORY I

L	T	P	C
0	0	4	3

1. Modeling of Sequential Digital system using VHDL.
2. Modeling of Sequential Digital system using Verilog.
3. Design and Implementation of ALU using FPGA.
4. Simulation of NMOS and CMOS circuits using SPICE.
5. Modeling of MOSFET using C.
6. Implementation of FFT- Digital Filters in DSP Processor.
7. Implementation of DSP algorithms using software package.
8. Implementation of MAC Unit using FPGA.

SEMESTER II

AN 5151 – ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS

L	T	P	C
3	0	0	3

UNIT I MODELS FOR INTEGRATED CIRCUIT ACTIVE DEVICES 9

Depletion region of a PN junction – Large signal behavior of Bipolar Transistors – Small Signal model of Bipolar Transistor – Large Signal behavior of MOSFET – Small Signal model of the MOS transistors – Short channel effects in MOS transistors – Weak inversion in MOS transistors – Substrate current flow in MOS transistor

UNIT II CIRCUIT CONFIGURATION FOR LINEAR IC 9

Current sources – Analysis of difference amplifiers with active load using BJT and FET – Supply and temperature independent biasing techniques – Voltage references. Output stages: Emitter follower – Source follower and Push pull output stages

UNIT III OPERATIONAL AMPLIFIERS 9

Analysis of Operational Amplifiers circuit – Slew rate model and high frequency analysis – Frequency response of integrated circuits: Single stage and multistage amplifiers – Operational Amplifier noise

UNIT IV ANALOG MULTIPLIER AND PLL 9

Analysis of four quadrants and variable trans conductance multiplier – Voltage Controlled Oscillator – closed loop analysis of PLL – Monolithic PLL design in integrated circuits: Sources of noise – Noise models of Integrated – Circuit Components – Circuit Noise Calculations – Equivalent Input Noise Generators – Noise Bandwidth – Noise – Figure and Noise Temperature

UNIT V ANALOG DESIGN WITH MOS TECHNOLOGY 9

MOS Current Mirrors – Simple – Cascode – Wilson and Widlar current source – CMOS Class AB output stages – Two stage MOS Operational Amplifiers – With Cascode – MOS Telescopic – Cascode Operational Amplifier – MOS Folded Cascode and MOS Active Cascode Operational Amplifiers

Total: 45

TEXT BOOKS

1. Gray- Meyer- Lewis- Hurst- “Analysis and design of Analog IC’s”- 4th Edition- Willey International- 2002.
2. Nandita Dasgupata- Amitava Dasgupta-”Semiconductor Devices-Modelling and Technology”- Prentice Hall of India Pvt.Ltd-2004.

REFERENCES

1. Behzad Razavi- “Principles of Data Conversion System Design”- S.Chand and Company Ltd,2000.
2. Grebene- Bipolar and MOS Analog Integrated Circuit Design”, John Wiley & sons, Inc., 2003.
3. Phillip E.Allen Douglas R. Holberg, “CMOS Analog Circuit Design”, Second Edition, Oxford University Press, 2003

VL 5151 – COMPUTER AIDED DESIGN OF VLSI CIRCUITS

L	T	P	C
3	0	0	3

UNIT I **9**

Introduction to VLSI Design Methodologies – Review of Data structures and algorithms – Review of VLSI Design automation tools – Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable problems – General purpose methods for Combinatorial Optimization

UNIT II **9**

Layout Compaction – Design rules – Problem formulation – Algorithms for Constraint Graph Compaction – Placement and partitioning – Circuit representation – Placement algorithms – Partitioning

UNIT III **9**

Floor Planning concepts – Shape functions and Floorplan sizing – Types of Local Routing problems – Area routing – Channel routing – Global routing – Algorithms for Global Routing

UNIT IV **9**

Simulation – Gate–level modeling and simulation – Switch–level modeling and simulation – Combinational Logic Synthesis – Binary Decision Diagrams – Two Level Logic Synthesis

UNIT V **9**

High level Synthesis – Hardware models – Internal representation – Allocation assignment and scheduling – Simple Scheduling algorithm – Assignment problem – High level transformations

Total: 45

TEXT BOOKS

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons-2002.
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation" Kluwar Academic Publishers- 2002.

REFERENCES

1. Christopher Michael and Mohammed Ismail , " Staistical Modelling of Computer Aided Design of MOS VLSI Circites", Kulwer Academic Publishers.
2. Drechsler R., "Evolutionary Algorithms for VLSI CAD", Kluwer Academic Publishers, 1998.
3. Hill- D.- D. Shugard J. Fishburn and K. Keutzer, "Algorithms and Techniques for VLSI Layout Synthesis", Kluwer Academic Publishers, 1989.

AN5152 – COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

L	T	P	C
3	0	0	3

UNIT I PRINCIPLES OF PARALLEL PROCESSING 9

Multiprocessors and Multicomputers – Multivector and SIMD Computers – PRAM and VLSI Models – Conditions of Parallelism – Program Partitioning and Scheduling –Program Flow mechanisms – Parallel Processing applications – Speed up Performance Law

UNIT II PROCESSOR AND MEMORY ORGANIZATION 9

Advanced Processor Technology – Superscalar and Vector Processors – Memory hierarchy technology – Virtual Memory technology – Cache Memory Organization – Shared Memory Organization

UNIT III PIPELINE AND PARALLEL ARCHITECTURE 9

Linear Pipeline Processors – Non Linear Pipeline processors – Instruction pipeline design – Arithmetic design – Superscalar and Super Pipeline design – Multiprocessor system interconnects – Message passing mechanisms

UNIT IV VECTOR– MULTITHREAD AND DATAFLOW ARCHITECTURE 9

Vector Processing principle – Multivector Multiprocessors – Compound Vector processing – Principles of Multithreading – Fine Grain Multicomputers – Scalable and Multithread Architectures – Dataflow and Hybrid Architectures

UNIT V SOFTWARE AND PARALLEL PROCESSING 9

Parallel programming models – Parallel languages and Compilers – Parallel programming environments – Synchronization and Multiprocessing modes – Message Passing program development – Mapping programs onto Multicomputers– Multiprocessor UNIX design goals – MACH/OS kernel architecture – OSF/1 architecture and applications

Total: 45

TEXT BOOK

1. Kai Hwang- Advanced Computer Architecture- TMH 2001**.**

REFERENCES

1. William Stallings, “Computer Organization and Architecture”, McMillan Publishing Company, 1990.
2. M.J. Quinn, “Designing efficient Algorithms for parallel computer”, McGraw Hill International, 1994.
3. Hesham E1-Rewini and Mostafa Abd-El-Barr, “Advanced Computer Architecture and Parallel Processing”, John Wiley and sons, 2005.

AN5154 – EMBEDDED SYSTEMS

L	T	P	C
3	0	0	3

UNIT I EMBEDDED ARCHITECTURE 9

Embedded Computers – Characteristics of Embedded Computing Applications – Challenges in Embedded Computing system design – Embedded System design process – Requirements – Specification – Architectural Design – Designing Hardware and Software Components – System Integration – Formalism for System Design – Structural Description – Behavioral Description – Design Example: Model Train Controller

UNIT II EMBEDDED PROCESSOR AND COMPUTING PLATFORM 9

ARM processor – processor and memory organization – Data operations – Flow of Control – SHARC processor – Memory organization – Data operations – Flow of Control – Parallelism with instructions – CPU Bus configuration – ARM Bus – SHARC Bus – Memory devices – Input/output devices – Component interfacing – designing with microprocessor development and debugging – Design Example : Alarm Clock

UNIT III NETWORKS 9

Distributed Embedded Architecture – Hardware and Software Architectures – Networks for Embedded Systems – I2C – CAN Bus – SHARC link p ports – Ethernet – Myrinet – Internet – Network–Based design – Communication Analysis – System Performance Analysis – Hardware platform design – Allocation and scheduling – Design Example: Elevator Controller

UNIT IV REAL–TIMECHARACTERISTICS 9

Clock driven Approach – Weighted Round Robin Approach– Priority driven Approach – Dynamic Versus Static systems – Effective release times and deadlines – Optimality of the Earliest Deadline First (EDF) algorithm – Challenges in validating timing constraints in priority driven systems – Off–line versus On–line scheduling

UNIT V SYSTEM DESIGN TECHNIQUES 9

Design Methodologies – Requirement Analysis – Specification – System Analysis and Architecture Design – Quality Assurance – Design Example: Telephone PBX – System Architecture – Ink jet printer – Hardware Design and Software Design – Personal Digital Assistants – Set–top Boxes

Total: 45

REFERENCES

1. Wayne Wolf “Computers as Components: Principles of Embedded Computing System Design**”,** Morgan Kaufman Publishers, 2001.
2. Jane.W.S., “ Liu Real-Time systems**”**, Pearson Education , 2000.
3. C. M. Krishna and K. G. Shin, “Real Time Systems”, McGraw Hill, 1997.
4. Frank Vahid and Tony Givargi, “Embedded System Design: A Unified Hardware/Software Introduction”, John Wiley & Sons, 2000.

VL5152 – VLSI DESIGN LABORATORY II

L	T	P	C
0	0	4	3

1. Implementation of 8 Bit ALU in FPGA / CPLD.
2. Implementation of 4 bit sliced processor in FPGA / CPLD.
3. Implementation of Elevator controller using embedded microcontroller.
4. Implementation of Alarm clock controller using embedded microcontroller.
5. Implementation of model train controller using embedded microcontroller.
6. System design using PLL.

ELECTIVES

VL5001 – TESTING OF VLSI CIRCUITS

L	T	P	C
3	0	0	3

UNIT I **9**

Introduction to Testing – Faults in digital circuits – Modeling of faults – Logical Fault Models – Fault detection – Fault location – Fault dominance – Logic Simulation – Types of simulation – Delay models – Gate level Event–driven simulation

UNIT II **9**

Test generation for Combinational Logic circuits – Testable Combinational Logic circuit design – Test generation for Sequential circuits – Design of testable Sequential circuits

UNIT III **9**

Design for Testability – Ad hoc design – Generic scan based design – Classical scan based design – System level DFT approaches

UNIT IV **9**

Built–In Self Test – Test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test algorithms – Test generation for Embedded RAMs

UNIT V **9**

Logic Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits – Self–checking design – System Level Diagnosis

Total: 45

TEXT BOOKS

1. M. Abramovici, M.A. Breuer and A.D. Friedman, “Digital Systems and Testable Design”, Jaico Publishing House, 2002.
2. P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002.

REFERENCES

1. M.L. Bushnell and V.D. Agrawal, “Essentials of Electronic Testing for Digital mory and Mixed Signal VLSI Circuits”, Kluwar Academic Publishers, 2002.
2. A.L. Crouch, “Design for Test for Digital IC's and Embedded Core Systems”, Prentice Hall International, 2002.
3. Nicolici Nicola and Al Hashimi Bashir M., “Power constrained Testing of VLSI Circuits”,Springer Publications.

VL5002 – LOW POWER VLSI DESIGN

L	T	P	C
3	0	0	3

UNIT I POWER DISSIPATION IN CMOS 9

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices – Basic principle of low power design

UNIT II POWER OPTIMIZATION 9

Logical level power optimization – Circuit level low power design – Circuit techniques for reducing power consumption in Adders and Multipliers

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS 9

Computer Arithmetic techniques for low power systems – Reducing power consumption in memories – Low power clock– Interconnect and layout design – Advanced techniques – Special techniques

UNIT IV POWER ESTIMATION 9

Power estimation techniques – Logic level power estimation – Simulation power analysis – Probabilistic power analysis

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER 9

Synthesis for low power –Behavioral level transforms – Software design for low power

Total: 45

TEXT BOOKS

1. K.Roy and S.C. Prasad, " LOW POWER CMOS VLSI circuit design", Wiley 2000.
2. Dimitrios Soudris, Chirstian Pignet and Costas Goutis, "Designing CMOS Circuits For Low Power", Kluwer, 2002.

REFERENCES

1. J.B. Kuo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley 1999.
2. A.P.Chandrakasan and R.W. Broadersen, "Low power digital CMOS design", Kluwer, 1995.
3. Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998.
4. Abdellatif Bellaouar, Mohamed.I. and Elmasry, " Low power digital VLSI design", Kluwer,2008
5. James B. Kuo and Shin chia Lin, "Low voltage SOI CMOS VLSI Devices and Circuits", John Wiley and sons, 2001.

VL5003 – VLSI SIGNAL PROCESSING

L	T	P	C
3	0	0	3

UNIT I FUNDAMENTAL TO DSP SYSTEMS 9

Introduction To DSP Systems – Typical DSP algorithms Iteration Bound – Data flow graph representations – Loop bound and Iteration bound – Longest path Matrix algorithm Pipelining and Parallel processing – Pipelining of FIR digital filters – Parallel processing – Pipelining and Parallel processing for low power

UNIT II RETIMING 9

Retiming – Definitions and properties Unfolding – An algorithm for Unfolding– properties of unfolding – Sample period reduction and parallel processing application Algorithmic strength reduction in filters and transforms – 2– parallel FIR filter – 2–parallel fast FIR filter – DCT algorithm architecture transformation – Parallel architectures for rank – Order filters – Odd – Even Merge – Sort architecture – Parallel rank – Order filters

UNIT III FAST CONVOLUTION 9

Fast Convolution – Cook – Toom algorithm – Modified Cook – Took Algorithm Pipelined and Parallel Recursive and adaptive filters – Inefficient/efficient single channel interleaving – Look – Ahead pipelining in first – Order IIR filters – Look – Ahead pipelining with power–of–two decomposition – Clustered Look–Ahead pipelining– parallel processing of IIR filters – Combined pipelining and parallel processing of IIR filters – Pipelined Adaptive Digital filters – Relaxed look–ahead – pipelined LMS Adaptive filter

UNIT IV BIT–LEVEL ARITHMETIC ARCHITECTURES 9

Scaling and round off noise – Scaling operation – Round off noise – State variable description of Digital filters – Scaling and round off noise computation – Round off noise in pipelined first – Order filters Bit – Level Arithmetic Architectures – Parallel multipliers with sign extension – Parallel carry – Ripple array multipliers – Parallel carry–save multiplier – 4x4 bit Baugh – Wooley carry – Save multiplication tabular form and implementation – Design of Lyon's bit – Serial multipliers using Horner's rule–bit – Serial FIR filter – CSD representation – CSD multiplication using Horner's rule for precision improvement

UNIT V PROGRAMMING DIGITAL SIGNAL PROCESSORS 9

Numerical Strength Reduction – Sub expression elimination – Multiple Constant multiplications – Iterative matching – Linear transformations Synchronous – Wave and Asynchronous pipelining – Synchronous pipelining and clocking styles – Clock skew in edge–triggered single–phase clocking – Two–phase clocking – Wave pipelining – Asynchronous pipelining bundled data versus dual rail protocol Programming Digital Signal Processors – General architecture with important features Low power design – Needs for low power VLSI chips – Charging and Discharging capacitance – Short – circuit current of an inverter – CMOS leakage current – Basic principles of low power design

Total: 45

TEXT BOOKS

1. Keshab K. Parhi, "VLSI Digital Signal Processing systems- Design and implementation",Wiley, Inter Science, 1999.
2. Gary Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Publishers, 1998.

REFERENCES

1. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing", Mc Graw Hill, 1994.
2. S.Y. Kung, H.J. White House and T. Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1985.
3. Jose E. France and Yannis Tsividis, "Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994.

VL5004 – CMOS VLSI DESIGN

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UNIT I MOS TRANSISTOR THEORY 9

Introduction to I.C Technology – Basic MOS transistors – Threshold Voltage – Body effect – Basic D.C. Equations – Second Order effects – MOS models – Small signal A.C characteristics – The complementary CMOS inverter – DC characteristics – Static Load MOS inverters – The Differential Inverters – Transmission gate

UNIT II CMOS PROCESSING TECHNOLOGY 9

Silicon semiconductor technology – Wafer processing – Oxidation – epitaxy – deposition – Ion implantation – CMOS technology – nwell – pwell process – Silicon insulator – CMOS process enhancement. Interconnect and circuit elements – Layout design rules – Latchup

UNIT III CIRCUIT CHARACTERISTICS AND PERFORMANCE ESTIMATION 9

Resistance estimation – Capacitance estimation – MOS capacitor characteristics – Device capacitances – Diffusion capacitance – SPICE modeling of MOS capacitance – Routing capacitance – Distributed RC effects – Inductance – Switching characteristics – Rise time – Fall time – Delay time – Empirical delay models – Gate delays – CMOS gate transistor sizing – Power dissipation – Scaling of MOS transistor dimensions

UNIT IV CMOS CIRCUIT AND LOGIC DESIGN 9

CMOS Logic gate design – Fan in and fan out – Typical CMOS NAND and NOR delays – Transistor sizing – CMOS logic structures – Complementary logic – BICMOS logic – Pseudo nMOS logic – Dynamic CMOS logic – Clocked CMOS logic – Pass transistor logic – CMOS domino logic – NP domino logic – Cascade voltage switch logic – Source follower pull up Logic (SFPL) – Clocking strategies – I/O structures

UNIT V CMOS SUBSYSTEM DESIGN 9

Data path operations – Addition/subtraction – Parity generators – Comparators – Zero/one detectors – Binary Counters – ALUs – Multiplication – Array – Radix–n – Wallace Tree and Serial Multiplication – Shifters – Memory elements – RWM Rom– Content Addressable Memory Control: FSM – PLA Control Implementation

Total: 45

TEXT BOOKS

1. Neil.H.E. Weste and K.Eshragian, “Principles of CMOS VLSI Design”, 2nd Edition, Addison. Wesley, 2000
2. Wayne Wolf, “Modern VLSI Design”, Pearson Education, 2002.

REFERENCES

1. Douglas a. Pucknell and K.Eshragian, “Basic VLSI Design”, 3rd Edition, PHI, 2000.
2. R. Jacob Baker, Harry W. LI. & David K. Boyce., “CMOS Circuit Design”, 3rd Indian reprint, PHI- 2000.
3. Neil Weste & David Hawis, “CMOS VLSI Design”, A Circuits and System Prospective, 3rd Edition
4. Jacob Baker, “CMOS Circuit Design: Layout and Simulation”, 2nd Edition, IEEE Press.

VL5005 – ANALOG VLSI DESIGN

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UNIT I BASIC CMOS CIRCUIT TECHNIQUES- CONTINUOUS TIME AND LOW-VOLTAGE SIGNAL PROCESSING 9

Mixed – Signal VLSI Chips – Basic CMOS Circuits – Basic Gain Stage – Gain Boosting Techniques – Super MOS Transistor – Primitive Analog Cells – linear voltage – Current Converters – MOS Multipliers and Resistors – CMOS – Bipolar and Low–Voltage BiCMOS Op–Amp Design– Instrumentation Amplifier Design – Low Voltage Filters

UNIT II BASIC BICMOS CIRCUIT TECHNIQUES– CURRENT –MODE SIGNAL PROCESSING AND NEURAL INFORMATION PROCESSING 9

Continuous – Time Signal Processing – sampled Data Signal Processing – Switched –Current Data Converters – Practical Considerations in SI Circuits Biologically –Inspired Neural Networks – Floating – Gate – Low–Power Neural Networks – CMOS Technology and Models – Design Methodology – Networks – Contrast Sensitive Silicon Retina

UNIT III SAMPLED–DATA ANALOG FILTERS– OVER SAMPLED A/D CONVERTERS AND ANALOG INTEGRATED SENSORS 9

First – order and Second SC Circuits – Bilinear Transformation – Cascade Design –Switched – Capacitor Ladder Filter – Synthesis of Switched – Current Filter – Nyquist rate A/D Converters – Modulators for Over sampled A/D Conversion – First and Second Order and Multibit Sigma–Delta Modulators – Interpolative Modulators –Cascaded Architecture – Decimation Filters – Mechanical – Thermal – Humidity and Magnetic Sensors – Sensor Interfaces

UNIT IV DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS 9

Fault modeling and Simulation – Testability – Analysis Technique – Ad Hoc Methods and General Guidelines – Scan Techniques – Boundary Scan – Built–in Self Test –Analog Test Buses – Design for Electron – Beam Testability – Physics of Interconnects in VLSI–Scaling of Interconnects – A Model for Estimating Wiring Density – A Configurable Architecture for Prototyping Analog Circuits

UNIT V STATISTICAL MODELING AND SIMULATION, ANALOG COMPUTER–AIDED DESIGN AND ANALOG AND MIXED ANALOG–DIGITAL LAYOUT 9

Review of Statistical Concepts – Statistical Device Modeling – Statistical Circuit Simulation – Automation Analog Circuit Design–automatic Analog Layout – CMOS Transistor Layout – Resistor Layout – Capacitor Layout–Analog Cell Layout – Mixed Analog – Digital Layout

Total: 45

TEXT BOOKS

1. Mohammed Ismail and Terri Fiez, " Analog VLSI signal and Information Processing ", McGraw Hill, International Editions, 1994.
2. Malcom R.Haskard and Lan C.May, "Analog VLSI Design NMOS and CMOS" , Prentice Hall India, 1998.

REFERENCES

1. Randall L Geiger and Phillip E. Allen, " Noel K.Strader VLSI Design Techniques for Analog and Digital Circuits", Mc Graw Hill, International Company, 1990.
2. Jose E.France and Yannis Tsividis, "Design of Analog Digital VLSI Circuits for Telecommunication and signal Processing", Prentice Hall, 1994.
3. Sina Balkin, Gunhan Dundar and A. Sekuk Orgrena, "Analog VLSI Design Automation", CRC Press.

VL5006 – DESIGN OF SEMICONDUCTOR MEMORIES

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UNIT I RANDOM ACCESS MEMORY TECHNOLOGIES STATIC RANDOM ACCESS MEMORIES (SRAMs) 9

SRAM Cell Structures – MOS SRAM Architecture – MOS SRAM Cell and Peripheral Circuit Operation – Bipolar SRAM Technologies – Silicon On Insulator (SOI) Technology – Advanced SRAM Architectures and Technologies – Application Specific SRAMs

DYNAMIC RANDOM ACCESS MEMORIES (DRAMs)

DRAM Technology Development – CMOS DRAMs – DRAMs Cell Theory and Advanced Cell Structures – BiCMOS – DRAMs – soft error failures in DRAMs –Advanced DRAM Designs and Architecture –Application Specific – DRAMs

UNIT II NONVOLATILE MEMORIES 9

Masked Read–Only Memories (ROMs) – High Density ROMs – Programmable Read –Only Memories (PROMs) – BipolarPROMs – CMOS PROMs – Erasable (UV) – Programmable Read–Only Memories (EPROMs) – Floating – Gate EPROM Cell–One Time Programmable (OTP) EPROM – Electrically Erasable PROMs (EEPROMs) –EEPROM Technology and Arcitecture – Nonvolatile SRAM – Flash Memories (EPROMs or EEPROM) – Advanced Flash Memory Architecture

UNIT III MEMORY FAULT MODELLING– TESTING– AND MEMORY DESIGN FORTESTABILITY AND FAULT TOLERANCE 9

RAM Fault Modelling – Electrical Testing – Peusdo Random Testing – Megabit DRAM Testing – Nonvolatile Memory Modelling and Testing – IDDQ Fault Modelling and Testing – Application Specific Memory Testing

UNIT IV SEMICONDUCTOR MEMORY RELIABILITY AND RADIATION EFFECTS 9

General Reliability Issues – RAM Failure Modes and Mechanism – Nonvolatile Memory Reliability – Reliability Modelling and Failure Rate Prediction – Design for Reliability – Reliability Test Structures – Reliability Screening and Qualification – RAM Fault Modelling – Electrical Testing – Peusdo Random Testing – Megabit DRAM Testing – Nonvolatile Memory Modelling and Testing – IDDQ Fault Modelling and Testing – Application Specific Memory Testing

UNIT V PACKAGING TECHNOLOGIES 9

Radiation Effects – Single Event Phenomenon (SEP) – Radiation Hardening Techniques – Radiation Hardening Process and Design Issues – Radiation Hardened Memory Characteristics – Radiation Hardness Assurance and Testing – Radiation Dosimetry – Water Level Radiation Testing and Test Structures – Ferroelectric Random Access Memories (FRAMs) – Gallium Arsenide (GaAs) FRAMs – Analog Memories – Magnetoresistive Random Access Memories (MRAMs) – Experimental Memory Devices – Memory Hybrids and MCMs (2D) – Memory Stacks and MCMs (3D)–Memory MCM Testing and Reliability Issues – Memory Cards – High Density Memory Packaging Future Directions

Total: 45

TEXT BOOKS

1. Ashok K. Sharma, “Semiconductor Memories: Technology, Testing and Reliability”, Wiley, IEEE Press, 2002.
2. Ashok K. Sharma, “Semiconductor Memories Two Volume Set”, Wiley, IEEE Press 2003.

REFERENCES

1. Ashok K. Sharma, “Semiconductor Memories: Technology Testing and Reliability Prentice Hall of India”, 1997.
2. Brent Keeth, R. Jacob Baker, “DRAM Circuit Design: A Tutorial”, Wiley, IEEE Press, 2000.
3. Betty Prince, **“**High Performance Memories: New Architecture DRAMs and SRAMs Evolution and Function”, Wiley,1999.

VL5007 – VLSI TECHNOLOGY

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UNIT I CRYSTAL GROWTH – WAFER PREPARATION– EPITAXY AND OXIDATION 9

Electronic Grade Silicon – Czochralski crystal growing – Silicon Shaping – Processing consideration – Vapor Phase Epitaxy – Molecular Beam Epitaxy – Silicon on Insulators – Epitaxial Evaluation – Growth Mechanism and Kinetics – Thin Oxides – Oxidation Techniques and Systems – Oxide properties – Redistridution of Dopants at interface – Oxidation of Poly Silicon – Oxidation inducted Defects.

UNIT I LITHOGRAPHY AND RELATIVE PLASMA ETCHING 9

Optical Lithography – Electron Lithography– X–Ray Lithography – Ion Lithography– Plasma properties – Feature Size control and Anisotropic Etch mechanism – Relative Plasma Etching techniques and equipments

UNIT III DEPOSITION – DIFFUSION – ION IMPLEMENTATION AND METALISATION 9

Deposition process– Polysilicon– Plasma assisted deposition– Models of Diffusion in Solids– Flick's one dimensional Diffusion Equation – Atomic Diffusion Mechanism – Measurement techniques – Range theory – Implant equipment. Annealing Shallow junction – High energy implantation – Physical vapour deposition – Patterning

UNIT IV PROCESS SIMULATION AND VLSI PROCESS INTEGRATION 9

Ion implantation – Diffusion and Oxidation – Epitaxy – Lithography – Etching and Deposition– NMOS IC Technology – CMOS IC Technology – MOS Memory IC technology – Bipolar IC Technology – IC Fabrication

UNIT V ANALYTICAL – ASSEMBLY TECHNIQUES AND PACKAGING OF VLSI DEVICES 9

Analytical Beams – Beams Specimen interactions – Chemical methods – Package types – Banking design consideration – VLSI Assembly technology – Package fabrication technology

Total: 45

TEXT BOOKS

1. S. M. Sze, "VLSI Technology", Mc.Graw.Hill, Second Edition, 1998.
2. Amar Mukherjee, "Introduction to NMOS and CMOS VLSI System design", 2000.

REFERENCES

1. James D Plummer, Michael D, Deal Peter B.Griffin,"Silicon VLSI Technology: Fundamentals, Practice and Modeling", 2000.
2. Wai Kai Chen, "VLSI Technology", CRC press, 2003.
3. James D. Plummer, Michael D. Deal, Peter B.Griffin, "Silicon VLSI Technology: Fundamentals, Practice and Modeling", Prentice Hall Electronics & VLSI series.

VL5008 – PHYSICAL DESIGN OF VLSI CIRCUITS

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UNIT I FUNDAMENTAL TO VLSI TECHNOLOGY 9

Layout Rules–Circuit abstraction Cell generation using Programmable Logic Array transistor chaining– Wein Berger arrays and gate matrices–layout of standard cells gate arrays and sea of gates–Field Programmable Gate Array(FPGA) – Layout methodologies – Packaging – Computational Complexity – Algorithmic Paradigms

UNIT II PLACEMENT USING TOP–DOWN APPROACH 9

Partitioning: Approximation of Hyper Graphs with Graphs– Kernighan–Lin Heuristic– Ratiocut– partition with capacity and i/o constraints – Floor planning: Rectangular dual floor planning – hierarchical approach – Simulated Annealing – Floor plan sizing – Placement: Cost function– Force Directed method – placement by Simulated Annealing – partitioning placement – module placement on a resistive network – Regular placement – Linear placement

UNIT III ROUTING USING TOP DOWN APPROACH 9

Fundamentals: Maze Running– Line Searching– Steiner Trees – Global Routing: Sequential Approaches– hierarchical approaches– multicommodity flow based techniques– Randomised Routing– One Step approach– Integer Linear Programming Detailed Routing: Channel Routing– Switch box routing. Routing in FPGA: Array based FPGA– Row based FPGAs

UNIT IV PERFORMANCE ISSUES IN CIRCUIT LAYOUT 9

Delay Models: Gate Delay Models– Models for Interconnected Delay– Delay in RC trees. Timing – Driven Placement: Zero Stack Algorithm– Weight based placement– Linear Programming Approach Timing Driving Routing: Delay Minimization– Click Skew Problem– Buffered Clock Trees. Minimization: Constrained via Minimization– Unconstrained via Minimization– Other issues in minimization

UNIT V SINGLE LAYER ROUTING- CELL GENERATION AND COMPACTION 9

Planar Subset Problem(PSP)– Single layer Global Routing– Single Layer Global Routing– Single Layer Detailed Routing– Wire Length and Bend Minimization technique – Over The Cell (OTC) Routing– Multiple Chip Modules(MCM)– Programmable Logic Arrays– Transistor Chaining– Wein Burger Arrays– Gate matrix layout– 1D Compaction– 2D Compaction

Total: 45

TEST BOOKS

1. Sarafzadeh C.K. Wong, "An Introduction to VLSI Physical Design", Mc Graw Hill International Edition, 1995
2. Preas M. Lorenzatti, " Physical Design and Automation of VLSI systems", The Benjamin Cummins Publishers, 1998.

REFERENCES

1. Ban Wong, Anurag Mittal, Yu Cao and Greg Starr, "Nano CMOS Circuit and Physical Design", Wiley John & Sons Incorporated, 2004.
2. Naveed A. Sherwani "Algorithm for VLSI Physical Design Automation", 3rd Edition, Springer, 1998.
3. Sadiq M. Sait, Habib Youssef, "VLSI Physical Design Automation– Theory and Practice",World Scientific Publishing Company, 1st Edition, 1999.
4. Bryan T. Preas, "Physical Design Automation of VLSI system", Michael Lorenzetti publisher, Benjamin Cummings Pub Co, 1998.

VL5009 – GENETIC ALGORITHMS AND THEIR APPLICATIONS

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UNIT I **9**

Introduction–GA Technology–Steady State Algorithm–Fitness Scaling–Inversion

UNIT II **9**

GA for VLSI Design– Layout and Test automation– Partitioning–Automatic Placement–Routing technology–Mapping for FPGA– Automatic test generation– Partitioning Algorithm Taxonomy–Multiway Partitioning

UNIT III **9**

Hybrid Genetic – Genetic Encoding–Local Improvement–WDFR–Comparison of Cas– Standard cell placement–GASP algorithm–Unified Algorithm

UNIT IV **9**

Global Routing–FPGA technology Mapping–Circuit generation–test generation in a GA frame work–test generation procedures

UNIT V **9**

Power Estimation–Application of GA–Standard cell placement–GA for ATG–Problem Encoding–Fitness function–GA vs Conventional algorithm.

Total: 45

TEXT BOOK

1. Pinaki Mazumder, E.MRudnick", Genetic Algorithm for VLSI Design Layout and test Automation", Prentice Hall, 1998.

REFERENCES

1. Randy L. Haupt, Sue Ellen Haupt, "Practical Genetic Algorithms", Wiley, Interscience, 1977.
2. Ricardo Sal Zebulum, Macro Aurelio Pacheco and Marley Maria Vellasco- "Evolution Electronics: Automatic Design of electronic Circuits and Systems Genetic Algorithms"- CRC press- 1st Edition Dec 2001.
3. John R.Koza, Forrest H. and Bennett David Andre, "Genetic Programming Automatic Programming and Automatic Circuit Synthesis", Morgan Kufmann, 1st Edition, May 1999.

AN5104 – ADVANCED MICROPROCESSORS AND MICRO CONTROLLERS

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UNIT I MICROPROCESSOR ARCHITECTURE 9

Instruction set - Data formats – Instruction formats – Addressing Modes – Memory hierarchy – register file – Cache – Virtual memory and paging – Segmentation – Pipelining – The instruction pipeline – pipeline hazards – Instruction level parallelism – reduced instruction set – Computer principles – RISC versus CISC – RISC properties – RISC evaluation – On–chip register files versus cache evaluation

UNIT II HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM 9

The software model – Functional description – CPU pin descriptions – RISC concepts – Bus operations – Super Scalar architecture – Pipelining – Branch prediction – The instruction and caches – Floating point unit –protected mode operation – Segmentation – Paging – Protection – Multitasking – Exception and Interrupts – Input /Output – Virtual 8086 model – Interrupt Processing –Instruction types – Addressing modes – Processor flags – Instruction set –programming the Pentium processor

UNIT III HIGH PERFORMANCE RISC ARCHITECTURE: ARM 9

The ARM architecture – ARM Assembly Language Program – ARM Organization and implementation – The ARM instruction set – The Thumb instruction set – ARM CPU cores

UNIT IV MOTOROLA 68HC11 MICROCONTROLLERS 9

Instructions and addressing modes – operating modes – Hardware reset – Interrupt system – Parallel I/O ports – Flags – Real time clock – Programmable timer – pulse accumulator – serial communication interface – A/D converter – hardware expansion – Assembly language Programming

UNIT V PIC MICRO CONTROLLER 9

CPU architecture – Instruction set – Interrupts – Timers – I/O port expansion –I^2C bus for peripheral chip access – A/D converter – UART

Total: 45

TEXT BOOKS

1. Daniel Tabak , “ Advanced Microprocessors”, McGraw Hill.Inc.- 1995
2. Steve Furber , “ ARM System -On-Chip architecture”, Addison Wesley - 2000.
3. John .B.Peatman , “ Design with PIC Microcontroller”, Prentice hall- 1997.
4. Valvano, “Embedded Microcomputer Systems”, Thomson Asia PVT LTD, First reprint 2001.

REFERENCES

1. James L. Antonakos , “ The Pentium Microprocessor”, Pearson Education , 1997.
2. Gene .H.Miller , “ Micro Computer Engineering”, Pearson Education, 2003.
3. James L.Antonakos, “An Introduction to the Intel family of Microprocessors”, Pearson Education, 1999.
4. Barry.B.Breg, “The Intel Microprocessors Architecture - Programming and Interfacing”, PHI, 2002.

Web links

www.ocw.nit.edu

www.arm.com

AN5002 – NEURAL NETWORKS AND APPLICATIONS

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UNIT I BASIC LEARNING ALGORITHM 9

Biological Neuron – Artificial Neural Model – Types of activation functions – Architecture: Feed forward and Feedback – Learning Process: Error Correction Learning –Memory Based Learning – Hebbian Learning – Competitive Learning – Boltzman Learning – Supervised and Unsupervised Learning – Learning Tasks: Pattern Space – Weight Space – Pattern Association – Pattern Recognition – Function Approximation – Control – Filtering – Beam forming – Memory – Adaptation – Statistical Learning Theory – Single Layer Perceptron – Perceptron Learning Algorithm – Perceptron Convergence Theorem – Least Mean Square Learning Algorithm – Multilayer Perceptron – Back Propagation Algorithm – XOR problem – Limitations of Back Propagation Algorithm

UNIT II RADIAL–BASIS FUNCTION NETWORKS AND SUPPORT VECTOR MACHINES: RADIAL BASIS FUNCTION NETWORKS: 9

Cover's Theorem on the Separability of Patterns – Exact Interpolator – Regularization Theory – Generalized Radial Basis Function Networks – Learning in Radial Basis Function Networks – Applications: XOR Problem – Image Classification

SUPPORT VECTOR MACHINES:

Optimal Hyperplane for Linearly Separable Patterns and Nonseparable Patterns – Support Vector Machine for Pattern Recognition – XOR Problem – □–insensitive Loss Function – Support Vector Machines for Nonlinear Regression

UNIT III COMMITTEE MACHINES 9

Ensemble Averaging – Boosting – Associative Gaussian Mixture Model – Hierarchical Mixture of Experts Model (HME) – Model Selection using a Standard Decision Tree – A Priori and post priori Probabilities – Maximum Likelihood Estimation – Learning Strategies for the HME Model – EM Algorithm – Applications of EM Algorithm to HME Model

NEURODYNAMICS SYSTEMS: Dynamical Systems – Attractors and Stability – Non–linear Dynamical Systems – Lyapunov Stability – Neurodynamical Systems – The Cohen–Grossberg Theorem

UNIT IV ATTRACTOR NEURAL NETWORKS 9

Associative Learning – Attractor Neural Network Associative Memory – Linear Associative Memory – Hopfield Network – Content Addressable Memory – Strange Attractors and Chaos – Error Performance of Hopfield Networks – Applications of Hopfield Networks – Simulated Annealing – Boltzmann Machine – Bidirectional Associative Memory – BAM Stability Analysis – Error Correction in BAMs – Memory Annihilation of Structured Maps in BAMS – Continuous BAMs – Adaptive BAMs – Applications

ADAPTIVE RESONANCE THEORY:

Noise–Saturation Dilemma – Solving Noise–Saturation Dilemma – Recurrent On–center –Off–surround Networks – Building Blocks of Adaptive Resonance – Substrate of Resonance Structural Details of Resonance Model – Adaptive Resonance Theory – Applications

UNIT V SELF ORGANISING MAPS 9

Self–organizing Map – Maximal Eigenvector Filtering – Sanger's Rule – Generalized Learning Law – Competitive Learning – Vector Quantization – Mexican Hat Networks – Self–organizing Feature Maps – Applications

PULSED NEURON MODELS: Spiking Neuron Model – Integrate–and–Fire Neurons – Conductance Based Models – Computing with Spiking Neurons

Total: 45

TEXT BOOKS

1. Satish Kumar, "Neural Networks: A Classroom Approach", Tata McGraw, Hill Publishing Company Limited,2004.
2. Simon Haykin, "Neural Networks: A Comprehensive Foundation", 2nd edition, Addison Wesley Longman (Singapore) Private Limited, 2001.

REFERENCES

1. Martin T.Hagan, Howard B. Demuth and Mark Beale, "Neural Network Design"- Thomson Learning, 2003.
2. James A, Freeman and David M. Skapura, "Neural Networks Algorithms Applications and Programming Techniques", Pearson Education (Singapore) Private Limited, 2003.

AN5005 – ASIC DESIGN

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UNIT I FUNDAMENTAL TO ASICS- CMOS LOGIC AND ASIC LIBRARY DESIGN 9

Types of ASICs – Design flow – CMOS transistors, CMOS Design rules – Combinational Logic Cell – Sequential logic cell – Data path logic cell – Transistors as Resistors – Transistor Parasitic Capacitance– Logical effort –Library cell design – Library architecture

UNIT II PROGRAMMABLE ASICS– PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS 9

Anti fuse – static RAM – EPROM and EEPROM technology – PREP benchmarks – Actel ACT – Xilinx LCA –Altera FLEX – Altera MAX DC & AC inputs and outputs – Clock & Power inputs – Xilinx I/O blocks

UNIT III PROGRAMMABLE ASIC INTERCONNECT– PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY 9

Actel ACT –Xilinx LCA – Xilinx EPLD – Altera MAX 5000 and 7000 – Altera MAX 9000 – Altera FLEX –Design systems – Logic Synthesis – Half gate ASIC –Schematic entry – Low level design language – PLA tools –EDIF– CFI design representation

UNIT IV LOGIC SYNTHESIS, SIMULATION AND TESTING 9

Verilog and logic synthesis –VHDL and logic synthesis – types of simulation –boundary scan test – fault simulation – automatic test pattern generation

UNIT V ASIC CONSTRUCTION– FLOOR PLANNING– PLACEMENT AND ROUTING 9

System partition – FPGA partitioning – Partitioning methods – Floor planning – placement – Physical design flow – Global routing – Detailed routing – Special routing – Circuit extraction – DRC

Total: 45

TEXT BOOKS

1. M. J. S. Smith, “Application Specific Integrated Circuits”, Addison Wesley Longman Inc.,1997.
2. Farzad Nekoogar and Faranak Nekoogar, “From ASICs to SOCs: A Practical Approach”, Prentice Hall PTR, 2003.

REFERENCES

1. Wayne Wolf, “FPGA-Based System Design”, Prentice Hall PTR, 2004.
2. R. Rajsuman, “System-on-a-Chip Design and Test”, Santa Clara- CA: Artech House Publishers, 2000.
3. F. Nekoogar, “Timing Verification of Application-Specific Integrated Circuits (ASICs) ”, Prentice Hall PTR- 1999.

AN5007 – RELIABILITY ENGINEERING

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UNIT I PROBABILITY PLOTTING AND LOAD-STRENGTH INTERFERENCE 9

Statistical Distribution – Statistical Confidence and Hypothesis testing – Probability plotting techniques – Weibull Extreme value Hazard – Binomial data – Analysis of load – strength interference – Safety margin and loading roughness on reliability

UNIT II RELIABILITY PREDICTION, MODELLING AND DESIGN 9

Statistical design of experiments and analysis of Variance Taguchi Method – ReliabilityPprediction – Reliability Modeling – Block diagram and Fault tree Analysis –Petri Nets – State space Analysis – Monte Carlo simulation – Design analysis methods – Quality function deployment – Load strength analysis – Failure modes – Effects and criticality analysis

UNIT III ELECTRONICS AND SOFTWARE SYSTEMS RELIABILITY 9

Reliability of electronic components – Component types and failure mechanisms – Electronic system reliability prediction – Reliability in electronic system design software errors – Software structure and modularity – Fault tolerance – Software reliability – Prediction and measurement – Hardware/software interfaces.

UNIT IV RELIABILITY TESTING AND ANALYSIS 9

Test environments – Testing for reliability and durability – Failure reporting – Pareto analysis – Accelerated Test Data Analysis – CUSUM charts – Exploratory Data analysis and Proportional Hazards Modeling – Reliability demonstration – Reliability growth monitoring.

UNIT V MANUFACTURE AND RELIABILITY MAQNAGEMENT 9

Control of Production Variability – Acceptance sampling – Quality control and Stress screening – Production failure reporting preventive maintenance strategy – Maintenance schedules – Design for Maintainability – Integrated Reliability programmes – Reliability and costs – Standard for reliability – Quality and safety – specifying reliability – Organization for reliability

Total: 45

TEXT BOOKS

1. Patrick D.T. O'Connor, David Newton and Richard Bromley, "Practical Reliability Engineering", Fourth edition, John Wiley & Sons, 2002.
2. David J. Klinger, Yoshinao Nakada , Maria A. Menendez and Von Nostrand Reinhold, New "AT & T Reliability Manual", 5th Edition, 1998.

REFERENCES

1. Gregg K. Hobbs, "Accelerated Reliability Engineering - HALT and HASS", John Wiley & Sons, 2000.
2. Lewis, "Introduction to Reliability Engineering", 2nd Edition, Wiley International, 1996.

AN5009 – SELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY IN SYSTEM DESIGN

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UNIT I EMI ENVIRONMENT 9

EMI/EMC concepts and definitions – Sources of EMI – conducted and radiated EMI – Transient EMI – Time domain Vs Frequency domain EMI – Units of measurement parameters – Emission and immunity concepts – ESD

UNIT II EMI COUPLING PRINCIPLES 9

Conducted – Radiated and Transient Coupling – Common Impedance Ground Coupling – Radiated Common Mode and Ground Loop Coupling – Radiated Differential Mode Coupling – Near Field Cable to Cable Coupling – Power Mains and Power Supply coupling

UNIT III EMI/EMC STANDARDS AND MEASUREMENTS 9

Civilian standards – FCC – CISPR – IEC – EN – Military standards – MIL STD 461D/462 – EMI Test Instruments /Systems – EMI Shielded Chamber – Open Area Test Site – TEM Cell – Sensors/Injectors/Couplers – Test beds for ESD and EFT – Military Test Method and Procedures (462)

UNIT IV EMI CONTROL TECHNIQUES 9

Shielding – Filtering – Grounding – Bonding – Isolation Transformer – Transient Suppressors – Cable Routing – Signal Control – Component Selection and Mounting

UNIT V EMC DESIGN OF PCB 9

PCB Traces Cross Talk – Impedance Control – Power Distribution Decoupling –Zoning – Motherboard Designs and Propagation Delay Performance Models

Total: 45

TEXT BOOKS

1. Henry W.Ott, “Noise Reduction Techniques in Electronic Systems”, John Wiley and Sons,1988
2. C.R.Paul, “Introduction to Electromagnetic Compatibility”, John Wiley and Sons, Inc., 1992.

REFERENCES

1. V. P. Kodali, “Engineering EMC Principles Measurements and Technologies”, IEEE Press, 1996.
2. Bernhard Keiser, “Principles of Electromagnetic Compatibility”, Artech house 3rd Edition 1986.

CO5006 – SPEECH AND AUDIO SIGNAL PROCESSING

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UNIT I MECHANICS OF SPEECH 9

Speech production mechanism – Nature of Speech signal – Discrete time modeling of speech production – Representation of Speech signals – Classification of Speech sounds – Phones – Phonemes – Phonetic and Phonemic alphabets – Articulatory features – Music production – Auditory perception – Anatomical pathways from the ear to the perception of sound – Peripheral auditory system – Psycho acoustics

UNIT II TIME DOMAIN METHODS FOR SPEECH PROCESSING 8

Time Domain parameters of Speech signal – Methods for extracting the parameters Energy – Average Magnitude – Zero Crossing Rate – Silence Discrimination using ZCR and energy – Short Time Auto Correlation Function – Pitch period estimation using Auto Correlation Function

UNIT III FREQUENCY DOMAIN METHOD FOR SPEECH PROCESSING 9

Short Time Fourier analysis – Filter bank analysis – Formant extraction – Pitch Extraction – Analysis by Synthesis – Analysis synthesis systems – Phase vocoder –Channel Vocoder

HOMOMORPHIC SPEECH ANALYSIS: Cepstral analysis of Speech – Formant and Pitch Estimation – Homomorphic Vocoders

UNIT IV LINEAR PREDICTIVE ANALYSIS OF SPEECH 9

Formulation of Linear Prediction problem in Time Domain – Basic Principle – Auto correlation method – Covariance method – Solution of LPC equations – Cholesky method – Durbin's Recursive algorithm – Lattice formation and solutions – Comparison of different methods – Application of LPC parameters – Pitch detection using LPC parameters – Formant analysis – VELP – CELP.

UNIT V APPLICATION OF SPEECH & AUDIO SIGNAL PROCESSING 10

Algorithms: Spectral Estimation – Dynamic time warping – Hidden Markov model – Music analysis – Pitch Detection – Feature analysis for recognition – Music synthesis – Automatic Speech Recognition – Feature Extraction for ASR – Deterministic sequence recognition – Statistical Sequence recognition – ASR systems – Speaker identification and verification – Voice response system – Speech Synthesis: Text to speech– voice over IP

Total: 45

TEXT BOOKS

1. Ben Gold and Nelson Morgan, "Speech and Audio Signal Processing", John Wiley and Sons Inc.,2004
2. L.R.Rabiner and R.W.Schaffer, "Digital Processing of Speech signals" Prentice Hall , 1978

REFERENCES

1. Quatieri , "Discrete-time Speech Signal Processing", Prentice Hall, 2001.
2. J.L.Flanagan, "Speech analysis: Synthesis and Perception, 2nd edition, 1972.
3. I.H.Witten, "Principles of Computer Speech", Academic Press, 1982.

CO5004 – DSP PROCESSOR ARCHITECTURE AND PROGRAMMING

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UNIT I FUNDAMENTALS OF PROGRAMMABALE DSPs 9

Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in P–DSPs – Multiple Access Memory – Multi–port memory – VLIW architecture– Pipelining – Special Addressing modes in P–DSPs – On chip Peripherals

UNIT II TMS320C5X PROCESSOR 9

Architecture – Assembly language syntax – Addressing modes – Assembly language Instructions – Pipeline structure– Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals

UNIT III TMS320C3X PROCESSOR 9

Architecture – Data formats – Addressing modes – Groups of Addressing Modes– Instruction sets – Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals – Generating and finding the sum of series – Convolution of two sequences – Filter design

UNIT IV ADSP PROCESSORS 9

Architecture of ADSP–21XX and ADSP–210XX series of DSP processors – Addressing modes and assembly language instructions – Application programs – Filter design – FFT calculation

UNIT V ADVANCED PROCESSORS 9

Architecture of TMS320C54X: Pipe line operation – Code Composer studio – Architecture of TMS320C6X – Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors

Total: 45

TEXT BOOK

1. B.Venkataramani and M.Bhaskar, “Digital Signal Processors – Architecture– Programming and Applications”, Tata McGraw Hill, Publishing Company Limited, 2003.

REFERENCES

1. User guides, Texas Instrumentation Analog Devices, Motorola.
2. Phil Lapsley, Jeff Bier, Amit Shoham and Edward A. Lee, “ DSP Processor Fundamentals – Architecture and Features”, Wiley IEEE Press.

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